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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
08/992,222	12/17/97	HOBBS	W	INPA:056

TM11/1024

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EXAMINER	
WILEY,D	
ART UNIT	**PAPER NUMBER**
2155	5

DATE MAILED: 10/24/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
08/992,022	Hobbs et al
Examiner	**Group Art Unit**
Wiley	2155

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on 8/13/00.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1, 3-24, 29-33 is/are pending in the application.

Of the above claim(s)_____ is/are withdrawn from consideration.

☐ Claim(s)_____ is/are allowed.

☒ Claim(s) 1, 3-24, 29-33 is/are rejected.

☐ Claim(s)_____ is/are objected to.

☐ Claim(s)_____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on_____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on_____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

DAVID A. WILEY
2155

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number)_____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received:_____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s)._____

☐ Interview Summary, PTO-413

☐ Notice of References Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other_____

Office Action Summary

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4-6 and 9-24, 29-33 are rejected under 35 U.S.C. 103(a) as being obvious over Gates (5,701,409).

   a. As for claims 1, 16, 21, 22 and 29-33, Gates teaches a system to test a bus comprising at least one instruction memory to store a predefined bus stimuli instruction and at least one phase generator coupled between the bus and the instruction memory for providing signals to the bus in response to the predefined bus stimuli instruction (abstract) but fails to teach storing more than one command.

Official Notice is taken with regards to the stroing of multiple commands in an instruction memory for the prurpose of speeding up the time needed to process instructions.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an istruction memory for multiple instruction, in Gates, to speed up processing.

b. As for claim 4, it is inherently seen that the IC (phase generator) can also receive signals from the bus.

c. As for claims 5, 17 and 23, it is inherently seen that some type of storing of predefined responses must be included for the device to compare results to detect errors.

d. As for claims 6 and 18, Gates teaches the phase generator includes one digital logic device responsive to the instructions and one phase engine for controlling timing (abstract; col. 2, lines 40-45).

e. As for claims 9 and 19, Gates teaches a control portion and data portion (col. 5, lines 27-45).

f. As for claim 10, Gates inherently teaches the control portion includes a flow logic device.

g. As for claim 11, Gates inherently teaches the phase engine includes at least on logic level translation device.

h. As for claim 12, it is inherently seen that these phases are included since a PCI bus includes these phases.

i. As for claims 13, 14, 20 and 24, Gates teaches a data memory coupled to the data portion and that the data portion receives data from the bus (col. 5, lines 27-45).

j. As for claim 15, Gates teaches a system to test a bus comprising at least one instruction memory to store a predefined bus stimuli instruction and at least one phase generator coupled between the bus and the instruction memory for providing signals to the bus in response to the predefined bus stimuli instruction (abstract). It is inherently seen that the IC (phase generator) can also receive signals from the bus. It is inherently seen that some type of storing of predefined responses must be included for the device to compare results to detect errors. Gates teaches the phase generator includes one digital logic device responsive to the instructions and one phase engine for controlling timing (abstract; col. 2, lines 40-45). Gates teaches a control portion and data portion (col. 5, lines 27-45). Gates inherently teaches the control portion includes a flow logic device. Gates inherently teaches the phase engine includes at least on logic level translation device. Gates teaches a data memory coupled to the data portion and that the data portion receives data from the bus (col. 5, lines 27-45).

4. Claims 3, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gates (5,701,409).

a. As for claim 3, Gates inherently teaches the instruction comprises an instruction word (col. 2, lines 40-45). Gates doesn't teach that the instruction word has a predefined length. Official Notice is taken that instruction words of predefined lengths are well known in the art. It would have been obvious to a person of ordinary skill in the art, at the time of the invention, to have used instruction words of any length because they are only a matter of computer design.

b. As for claims 7 and 8, Gates doesn't teach what the digital logic device comprises. Official Notice is taken that FPGA's and ASIC's are well known in the art. It would have been obvious to a person of ordinary skill in the art, at the time of the invention, to have used instruction words of any length because they are only a matter of computer design.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Wiley whose telephone number is (703) 308-5221. The examiner can normally be reached on Monday thru Friday from 7:00 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R. Sheikh, can be reached on (703) 305-9648. The fax phone number for this Group is (703) 305-3718.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [**ayza.sheikh@uspto.gov**].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-9600.

David A. Wiley

October 23, 2000